

Appl. No.: 09/652,322
Amdt. dated March 25, 2004
Reply to Office action of January 20, 2004

REMARKS/ARGUMENTS

Applicants received the Office Action dated January 20, 2004, in which the Examiner: (1) objected to informalities in the specification; (2) rejected claims 1-5, 13-14 and 22-24 as obvious in view of Passint et al. (US Patent No. 5,970,232 hereinafter referred to as "Passint") and Gotwald (US Patent No. 5,987,518); and (3) rejected claims 6-12 and 15-21 as obvious in view of Passint, Gotwald, and Miller et al. (US Patent No. 6,282,195). In this Response, Applicants amend claims 1-3, 14 and 23. Applicants also add claims 25-29. Claims 1-29 are pending. Based on the arguments and amendments contained herein, Applicants respectfully request reconsideration and allowance of the pending claims.

I. CLAIM REJECTIONS

A. CLAIM 1

Claim 1 was amended to clarify that the preamble language "with a plurality of microprocessors, which comprise" is intended as a limitation. Therefore, Applicants replaced the above preamble language with the limitation "a plurality of microprocessor units coupled to each other, wherein each microprocessor unit comprises." Applicants believe that the scope of claim 1 remains unchanged by the amendment.

Amended claim 1 requires "a plurality of microprocessor units, wherein each microprocessor unit comprises...a router to route message packets between said microprocessor units, and wherein said router prioritizes message packets based upon type of message packet, age of the message packet, and source of the message packet." Claim 1 further requires that each microprocessor unit comprise "a plurality of network input ports and network output ports connecting said plurality of microprocessor units to form a computer network, wherein each of said network input ports couples to one or more associated local arbiters in the router, each of said local arbiters operable to select a message packet among message packets waiting at the network input port."

Neither Passint nor Gotwald teaches or suggests the above limitations. Specifically, Passint teaches a multi-node system wherein each node (e.g., nodes

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22 and 24) comprises at least one processor and one memory (see Fig. 1 and col. 3, lines 15-20). Passint further teaches that the nodes 22, 24 are coupled to a router 28 via interface chips 34 and 34'. However, Passint does not disclose what is in the processors 131-134. Therefore, Applicants submit that the multi-node structure described in Passint does not teach "a plurality of microprocessor units, wherein each microprocessor unit comprises...a router" and "network input ports and network output ports."

It may be that the Examiner regards each multiprocessor node taught in Passint as one of the claimed "microprocessor units." In such case, Passint still does not teach that each multiprocessor node 1, 2 comprises a router as required in claim 1. Rather, Passint teaches that multiple nodes 22, 24 are connected to a single router or scalable interconnect network 28 (see Fig. 1). Furthermore, Passint teaches that the scalable interconnect network 28 "is independent of the complexity of the nodes 22, 24, and 26" (see col. 5, lines 35-45). Neither Passint nor Gotwald teaches or suggests "a plurality of microprocessor units, wherein each microprocessor unit comprises...a router" and "network input ports and network output ports" as required in claim 1. For at least these reasons, Applicants submit that claim 1 and all claims that depend from claim 1 are allowable.

B. CLAIM 14

Claim 14 was amended to clarify that the preamble language "to reduce routing latency" is intended as a limitation. Therefore, Applicants replaced the above preamble language with the limitation "wherein said selecting and said transmitting reduces routing latency of the distributed multiprocessing computer system." Applicants believe that the scope of claim 14 remains unchanged by the amendment.

Claim 14 requires "selecting a message packet at each of a plurality of microprocessor router input ports...based on the type of message packet" and "transmitting a message packet chosen from the selected...message packets...based on the microprocessor router input port priority, wherein said

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selecting and said transmitting reduces routing latency of the distributed multiprocessing computer system."

Neither Passint nor Gotwald teaches or suggests all of the above limitations. Gotwald teaches "priority can be based, for example, on the source address for the IP data, the destination IP address, the data type and/or the connection type." However, Gotwald does not teach that the priority "reduces routing latency of [a] distributed multiprocessing computer system" as required in claim 14. Rather, Gotwald teaches that the priority is used to "provide reserved bandwidth for broadcast services or to provide different levels of quality for specific IP addresses" (see col. 4, lines 55-58). For at least these reasons, Applicants submit that claim 14 and all claim that depend from claim 14 are allowable.

C. CLAIM 23

Claim 23 was amended to require "wherein [the] operation of said means for selecting and said means for transmitting reduces routing latency of the distributed multiprocessing computer system." As explained above, with respect to claim 14, neither Passint nor Gotwald teaches this limitation. For at least this reason, Applicants submit that claim 23 and claims that depend from claim 23 are allowable.

D. CLAIM 24

Claim 24, in part, requires "a plurality of microprocessors" which each comprise "a router to route message packets between said microprocessors," "a plurality of network input ports and network output ports connecting said plurality of microprocessors" and "a plurality of microprocessor input ports and microprocessor output ports that allow the exchange of message packets between hardware functional units in the microprocessor and between microprocessors."

Neither Passint nor Gotwald teaches or suggests all of these limitations. As explained above with respect to claim 1, neither Passint nor Gotwald teaches a microprocessor comprising "a router" and "a plurality of network input ports and network output ports." Furthermore, neither Passint nor Gotwald teaches or

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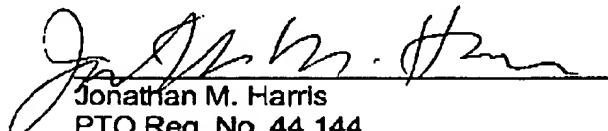
suggests "a plurality of microprocessor input ports and microprocessor output ports that allow the exchange of message packets between hardware functional units in the microprocessor and between microprocessors" as required in claim 24. For at least these reasons, Applicants submit that claim 24 and all claims that depend from claim 24 are allowable.

II. CONCLUSIONS

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the prior art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request that a timely Notice of Allowance be issued in this case. If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Respectfully submitted,



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